PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-230406

(43)Date of publication of application : 24.08.2001

----

(51)Int.Cl. H01L 29/762

H01L 21/339

H04N 5/335

----

(21)Application number : 2000-039937 (71)Applicant : NEC CORP

(22)Date of filing : 17.02.2000 (72)Inventor : NAKANO TAKASHI

----

(54) SOLID-STATE IMAGE SENSING DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a solid-state image sensing device with a high-gain source- follower-type amplifier where a power supply voltage VDD with a higher potential than a substrate voltage Vs is supplied.

SOLUTION: A first conductivity type semiconductor substrate 10 is connected to an approximately 5 V substrate voltage Vs. A second conductivity type region 11 is formed on the first conductivity type semiconductor substrate 10, a first conductivity type well 12 is formed in it, and a second conductivity well 13 is formed in it. In the second conductivity type well 13, a driver transistor Q13 is formed, and the well 13 is connected to a source diffusion layer 18a of the driver transistor Q13. In the second conductivity type region 11, a load transistor Q23 is formed and is connected to the ground. The first conductivity type well 12 is connected to an approximately 15 V power supply voltage VDD via a first conductivity type diffusion layer 16. The second conductivity type well 13 is

electrically separated from the first conductivity type well 12.

LEGAL STATUS [Date of request for examination] 16.01.2001

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 3591633

[Date of registration] 03.09.2004

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]

[Claim 1] In the solid state image sensor which has source follower mold amplifier The 1st conductivity-type substrate, it was formed in the 2nd conductivity-type field formed in said 1st conductivity-type substrate, and this 2nd conductivity-type field -- with a well and a load transistor the 1st conductivity type said 1st conductivity type -- a well -- the 2nd conductivity type formed inside -- a well and this 2nd conductivity type -- a well -- the solid state image sensor characterized by having the driver transistor formed inside and said load transistor and said driver transistor forming source follower mold amplifier.

[Claim 2] The source and said solid state image sensor according to claim 1 to which a well is connected the 2nd conductivity type of said driver transistor.

[Claim 3] The drain and said solid state image sensor according to claim 1 to which a well is connected the 1st conductivity type of said driver transistor.

[Claim 4] said solid state image sensor is equipped with three steps of source follower mold amplifier by which cascade connection was carried out, and the driver transistor of the source follower mold amplifier of the first rank is formed in said 2nd conductivity-type field -- having -- **** -- the driver transistor of the 2nd and the source follower mold amplifier of the 3rd step -- said 2nd conductivity type -- a well -- a solid state image sensor given in any of claims 1-3 which are characterized by being formed inside they are.

[Claim 5] A solid state image sensor given in any of claims 1-4 said driver transistor and said whose load transistor are a surface type or a pad mold they are.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a detail more about a solid state image sensor at the output amplifier section which has the buffer ability which amplifies the feeble electrical signal detected in the photo-electric-conversion section.

[0002]

[Description of the Prior Art] An MOS mold solid state image sensor is equipped with the image pick-up field section which changes light into a charge by photo electric conversion, the charge transfer section which transmits a charge, and the output amplifier section which transforms a charge into a predetermined voltage signal. The image pick-up field section generates the charge according to incident light with the photodiode by which a large number have been arranged for example, in the shape of an array. The output amplifier section is constituted as source follower mold amplifier with a low output impedance, and is carried on the same substrate with the image pick-up field section and the charge transfer section.

[0003] Drawing 5 (a) and (b) are the circuit diagrams and structural drawings of a solid state image sensor given in JP,60-223161,A. This drawing (a) is a circuit diagram of the output section which accomplishes source follower mold amplifier. Source follower mold amplifier has the driver transistor Q14 which was connected mutually at the serial and which inputs an electrical signal Si into the gate, and the load transistor Q24 which inputs bias voltage Vb into the gate. The driver transistor Q14 operates as a source follower mold amplifier, and commits the load transistor Q24 as a constant current source (source side resistance) of source follower mold amplifier.

[0004] This drawing (b) is a sectional view showing the structure of the output amplifier section of a solid state image sensor. A solid state image sensor is formed on the 1st conductivity-type (N type) semi-conductor substrate 10. The driver transistor Q14 is formed in the 2nd 2nd conductivity-type (P type) field 11 shown in the central site in drawing, and the load transistor Q24 is formed in the 1st 2nd conductivity-type (P type) field 11 shown in the left-hand side in drawing. The driver transistor Q14 and the load transistor Q24 constitute the source follower mold amplifier of this drawing (a).

[0005]

[Problem(s) to be Solved by the Invention] The technique given in the above-mentioned official report is raising the gain of source follower mold amplifier by connecting the source and the substrate of the driver transistor Q14.

[0006] Moreover, as the photodiode which a solid state image sensor has in an image pick-up field shows a good property, the substrate electrical potential difference Vs is supplied to the semi-conductor substrate 10, and supply voltage VDD is supplied to the drain side of source follower mold amplifier so that the linearity actuation [of source follower mold amplifier] range can be secured. Although the electrical potential difference of the substrate electrical potential difference Vs and supply voltage VDD was about 15V conventionally, current is holding down the substrate electrical potential difference Vs to about 5V with low-battery-izing which reduces power consumption.

[0007] The potential of the 2nd 2nd conductivity-type field 11 which it is maintained by about [of the intermediate voltage of supply voltage VDD] 7.5V, and is shown in the central site in drawing of source diffusion layer 18a of the driver transistor Q14 is the same as the potential of source diffusion layer 18a of the driver transistor Q14 so that source follower mold amplifier can secure a linearity operating range. Here, since, as for the 2nd 2nd conductivity-type field 11, about [2.5V] potential becomes high as compared with the 1st conductivity-type semi-conductor substrate 10 by holding down the substrate electrical potential difference Vs to about 5V for low-battery-izing, bias of the PN-junction side with the semi-conductor substrate 10 will be carried out to the forward direction. In this case, since the 2nd 2nd conductivity-type field 11 and 1st conductivity-type semi-conductor substrate 10 are not separated electrically, the function of the driver transistor Q14 is spoiled.

[0008] In case this invention is made in order to solve the trouble which a Prior art which was described above has, and it supplies the supply voltage VDD of high potential as compared with the substrate electrical potential difference Vs, it aims at offering a solid state image sensor equipped with the source follower mold amplifier of high interest profit which can supply a reverse bias electrical potential difference to a PN-junction side effectively.

[0009]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the solid state image sensor of this invention In the solid state image sensor which has source follower mold amplifier The 1st conductivity-type substrate, it was formed in the 2nd conductivity-type field formed in said 1st conductivity-type substrate, and this 2nd conductivity-type field -- with a well and a load transistor the 1st conductivity type said 1st conductivity type -- a well -- the 2nd conductivity type formed inside -- a well and this 2nd conductivity type -- a well -- it has the driver transistor formed inside and is characterized by said load transistor and said driver transistor forming source follower mold amplifier.

[0010] even if it makes the solid state image sensor of this invention lower than the supply voltage which supplies the substrate electrical potential difference supplied to the 1st conductivity-type semi-conductor substrate to the drain of a driver transistor, it is the source of a driver transistor -- since a well is electrically separated from the 1st conductivity-type semi-conductor substrate the 2nd conductivity type, it operates as source follower mold amplifier of high interest profit.
[0011] The source of said driver transistor, said thing [that a well is connected the 2nd conductivity type], or the drain of said driver transistor and said thing [that a well is connected the 1st conductivity type] of the solid state image sensor of this invention is desirable. In this case, a well is certainly separated electrically the 2nd conductivity type with a well the 1st conductivity type.
[0012] in the solid state image sensor of this invention, said solid state image sensor is equipped with three steps of source follower mold amplifier by which cascade connection was carried out, and the driver transistor of the source follower mold amplifier of the first rank is formed in said 2nd conductivity-type field -- having -- **** -- the driver transistor of the 2nd and the source follower mold amplifier of the 3rd step -- said 2nd conductivity type -- a well -- it can also be formed inside.
[0013] Moreover, said driver transistor and said load transistor of the solid state image sensor of this invention can also be a surface type or a pad mold.
[0014]
[Embodiment of the Invention] Hereafter, based on the example of an operation gestalt of this invention, the solid state image sensor of this invention is explained with reference to a drawing. Drawing 1 is the sectional view showing the structure of the solid state image sensor of the example of 1 operation gestalt of this invention. The solid state image sensor of this example of an operation gestalt has the image pick-up field section 102 which carries out photo electric conversion and generates an electrical signal, and the output amplifier section 101 which changes an electrical signal into a detecting signal, and is constituted on the 1st conductivity-type (N type) semi-conductor substrate 10. The 1st conductivity-type semi-conductor substrate 10 is connected to the about [5V] substrate electrical potential difference Vs. On the 1st conductivity-type semi-conductor substrate 10, the 2nd conductivity-type (P type) field 11 is formed, the 1st conductivity-type well 12 is formed in the 2nd conductivity-type field 11, and the 2nd conductivity-type well 13 is formed in the 1st conductivity-type well 12.
[0015] Drawing 2 is the circuit diagram of the output amplifier section 101 of drawing 1 . The source follower mold amplifier 3-5 of each stage is constituted considering the driver transistors Q11-Q13 of an n channel mold, and the load transistors Q21-Q23 of

an n channel mold as 1 set, respectively. All of the drain of the driver transistors Q11-Q13 are connected to the about [15V] supply voltage VDD. All of the gate of the load transistors Q21-Q23, the source, and a substrate are connected to a gland. The source of the driver transistors Q11-Q13 is connected to the drain of the corresponding load transistors Q21-Q23, respectively.

[0016] The gate is connected to an input terminal 1, a substrate is connected to a gland, and, as for the driver transistor Q11, the source is connected to the gate of the driver transistor Q12. As for the driver transistor Q12, the source is connected to the substrate and the gate of the driver transistor Q13. As for the driver transistor Q13, the source is connected to a substrate and an output terminal 2. It connects with the electrical signal output terminal of the image pick-up field section by which an input terminal 1 is not illustrated, and a solid state image sensor is connected to the signal input terminal of the external circuit where an output terminal 2 is not illustrated.

[0017] The driver transistors Q11-Q13 carry out low impedance conversion of the signal inputted into each gate, and output it as a signal of an inphase from the source. The load transistors Q21-Q23 operate as a constant current source to which the set-up fixed drain current flows, and between the drain sources becomes a high impedance seemingly. Amplification degree will become small if the source follower mold amplifier 3-5 has a small resisted part between the source of a driver transistor, and a gland. Between the source of a driver transistor, and a gland, when fixed resistance is connected as compared with the case where a constant current source is connected, the amplitude of the signal outputted from the source declines.

[0018] Drawing 3 is the sectional view showing the structure of the source follower mold amplifier 5 of drawing 2 . The 1st conductivity-type diffusion layer 16 constitutes the contact field for connecting with aluminum wiring, and is formed in the surface part on the 1st conductivity-type well 12. The 1st conductivity-type well 12 is connected to supply voltage VDD through the 1st conductivity-type diffusion layer 16. The driver transistor Q13 is a surface type with which it is formed on the 2nd conductivity-type well 13, and a channel does not exist beforehand. It is the pad mold with which the load transistor Q23 is formed on the 2nd conductivity-type field 11, and a channel exists beforehand as a 1st conductivity-type channel field 14, and all of the driver transistor Q11 and transistors other than Q13 are pad molds.

[0019] About all transistors, as for gate length and the design value of gate width, an optimum value is adopted, respectively so that the transistor characteristics of a band etc. may meet a design basis. Here, transistor structure will become the same if it specifies in any of a surface type or a pad mold it is.

[0020] Gate dielectric film consists of the structure of only silicon oxide, or the structure (ONO film) which sandwiched the silicon nitride film by silicon oxide. The gate electrodes 19a and 19b consist of polish recon, and are formed into low resistance like a metal by diffusing N type impurities, such as Lynn. The 1st conductivity-type diffusion layer 16, the source diffusion layers 18a and 18b, and the drain diffusion layers 17a and 17b are formed by doping N type impurities, such as Lynn. As for an ion implantation, impregnation concentration is performed to the order of one E12 to a P type field and an N type field, using the acceleration energy of hundreds keV(s) in both sides.
[0021] Drawing 4 is the top view showing the structure of the source follower mold amplifier 5 of drawing 2 . As for wiring 21-24, aluminum is used as a wiring material. Since contact 34 is connection with the field of P type, it is directly connected with the 2nd conductivity-type well 13. Contacts 31-33, and 35-38 are connections with an N type field, respectively, and they are connected through the diffusion layer into which the N type impurity was poured so that good ohmic contact may be obtained.
[0022] Here, the gain G of source follower mold amplifier is explained. If the conductance of gm and a substrate is set to gmb, it sets output conductance to gds1 for a mutual conductance to a driver transistor and source follower mold amplifier sets output conductance to gds2 to a load transistor, Gain G will be expressed by gm/(gm+gmb+gds1+gds2). If the substrate and the source of a driver transistor are connected, since gmb of an upper type will be set to 0, Gain G becomes high.
[0023] The channel combined with gate electrode 19a through gate oxide, and the channel has combined the driver transistor Q13 with the 2nd conductivity-type well 13 through a depletion layer [directly under]. Channel potential will be modulated if the driver transistor Q13 inputs a signal into gate electrode 19a. If the modulation of channel potential has the large mutual conductance gm which shows the degree of coupling of gate electrode 19a and a channel, it will be promoted, and if the conductance gmb of the substrate which shows the degree of coupling of the 2nd conductivity-type well 13 and channel which are fixed potential is small, it will be promoted.
[0024] the signal charge obtained by photo electric conversion in the solid state image sensor -- the first rank from ** suspension charge capacity and ** suspension charge capacity of the output section -- the wiring capacity to the driver transistor Q11, and ** -- the first rank -- since it changes into an electrical potential difference by the charge detection capacity which consists of the sum total of input-capacitance ** of the driver transistor Q11 and outputs through source follower amplifier, if charge detection

capacity is large, output voltage will decrease. the first rank -- if this invention is applied also to the source follower 3 -- the first rank -- although the gain G of the source follower 3 increases -- the first rank from suspension charge capacity -- since the wire length to the driver transistor Q11 is extended and charge detection capacity increases -- as output voltage -- the first rank -- the direction which does not apply this invention increases to the source follower 3 in many cases. therefore -- this example -- the first rank -- this invention is not applied to the source follower 3. The driver transistor Q11 makes the substrate the transistor structure linked to a gland. Moreover, when thinking improvement in Gain G as important, or when wiring capacity is small, the transistor structure where the substrate and the source of a driver transistor are connected is adopted to all the source follower mold amplifier 3-5.

[0025] The potential of the 1st conductivity-type well 12 is set to 15V, the potential of the 2nd conductivity-type well 13 is set to 7.5V, the potential of the 1st conductivity-type semi-conductor substrate 10 is set to 5V, and the potential of the 2nd conductivity-type field 11 is set to 0V. The reverse bias of all the PN-junction sides in which the 1st conductivity-type well 12, the 2nd conductivity-type well 13, the 1st conductivity-type semi-conductor substrate 10, and the 2nd conductivity-type field 11 are formed is carried out.

[0026] Since according to the above-mentioned example of an operation gestalt the 2nd conductivity-type well which is the source of a driver transistor is electrically separated from the 1st conductivity-type semi-conductor substrate even if it makes it lower than the supply voltage which supplies the substrate electrical potential difference supplied to the 1st conductivity-type semi-conductor substrate to the drain of a driver transistor, it operates as source follower mold amplifier of high interest profit.

[0027] In addition, although the above-mentioned example of an operation gestalt explained N channel transistor, if the conductivity type of an impurity is changed, effectiveness with the same said of a P channel transistor will be acquired. moreover, **** only whose driver transistors Q13 and Q23 are surface types in the above-mentioned example of an operation gestalt -- although it ******(ed) just, this invention is applicable also about the configuration each transistor is [configuration] in any of a surface type or a pad mold.

[0028] As mentioned above, although this invention was explained based on the suitable example of an operation gestalt, the solid state image sensor of this invention is not limited only to the configuration of the above-mentioned example of an operation gestalt, and the solid state image sensor which performed various corrections and modification from the configuration of the above-mentioned example of an operation

gestalt is also contained in the range of this invention.

[0029]

[Effect of the Invention] As explained above, since the 2nd conductivity-type well which is the source of a driver transistor is electrically separated from the 1st conductivity-type semi-conductor substrate even if it makes it lower than the supply voltage which supplies the substrate electrical potential difference supplied to the 1st conductivity-type semi-conductor substrate to the drain of a driver transistor, with the solid state image sensor of this invention, it operates as source follower mold amplifier of high interest profit. Moreover, since the substrate electrical potential difference to supply can be set up low, it can contribute to the cure against a low power.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view showing the structure of the solid state image sensor of the example of 1 operation gestalt of this invention.

[Drawing 2] It is the circuit diagram of the output amplifier section of the solid state image sensor of drawing 1 .

[Drawing 3] It is the sectional view showing the structure of the 3rd step source follower mold amplifier 5 of drawing 2 .

[Drawing 4] It is the top view showing the structure of the 3rd step source follower mold amplifier 5 of drawing 2 .

[Drawing 5] This drawing (a) and (b) are the circuit diagrams and structural drawings of

a solid state image sensor given in JP,60-223161,A.

[Description of Notations]

1 Input Terminal

2 Output Terminal

3 First Rank -- Source Follower Mold Amplifier

4 2nd Step Source Follower Mold Amplifier

5 3rd Step Source Follower Mold Amplifier

10 1st Conductivity-Type Semi-conductor Substrate (N Type)

11 2nd Conductivity-Type Field (P Type)

12 1st Conductivity-Type Well (N Type)

13 2nd Conductivity-Type Well (P Type)

14 1st Conductivity-Type Channel Field (N Type)

16 1st Conductivity-Type Diffusion Layer (N Type)

17a, 17b Drain diffusion layer (N type)

18a, 18b Source diffusion layer (N type)

19a, 19b Gate electrode

21-24 Wiring

31-38 Contact

Q11-Q14 Driver transistor (n channel mold)

Q21-Q24 Load transistor (n channel mold)

VDD Supply voltage

Vs Substrate electrical potential difference

Vb Bias voltage

Si Electrical signal

So Detecting signal